Creating a Circuit - Get New Part

1. Select the part to draw.
2. Choose 'Get New Part' from the toolbar.
Draw - Wire Components

Draw – Get New parts - Add Digital Signal Sources
Edit Attributes

Clock Attributes

- Name: DSTM5
- Specify by:
  - Frequency and duty cycle
  - Period and on time
- Frequency (Hz): 1000
- Duty cycle (%): 0.5
- Initial value: 0
- Time delay (sec): 0

OK Cancel Apply

Waveforms

Construct Circuit and Add V and I Markers
Analysis - Simulation Setup

The image shows a window titled "Analysis Setup" with several options. The enabled options include AC Sweep, Load Bias Point, Save Bias Point, DC Sweep, Monte Carlo/Worst Case, Bias Point Detail, and Digital Setup. There is also a checkbox for Transient analysis enabled. Below this window is another window titled "Transient" with fields for Start Time, End Time, No-Point Delay, and Step Cavity. There are options for Detailed Bias Pt, Skip initial transient solution, Enable Fourier, Center Frequency, Number of harmonics, and Output Var. The window has OK and Cancel buttons.

Analysis - Probe Setup

The image shows another window titled "Probe Setup Options" with tabs for Probe Startup, Data Collection, and Checkpoint. Under Probe Startup, there is an option for Auto-Run Option with sub-options for automatically running Probe after simulation, monitoring waveforms (auto-updated), and not auto-running Probe. Under At Probe Startup, there are options for Restore last Probe session, Show all markers, Show selected markers, and None. The window has OK and Cancel buttons.
Analysis - Simulate

Probe

Building Complex Pure Digital Circuits
Building Analog / Digital Circuits

For extra credit - Try your own circuits
Ideas to Implement the Design Labs

Note: These are only intended as ideas. They don’t necessarily represent the best way to implement the design.

Design Lab #1

Notes: Output of the flip-flop becomes the clock signal to the next one. The output of the following flip-flop becomes half the frequency of the previous one. The AND gates allow the switches to decide if the light will function.

Design Lab #2

Notes: The second pattern is just half the frequency of the first pattern. The third pattern will be a zero when patterns one and two are both zero. The XOR’s only allow one pattern to be shown at a time.
Design Lab #3

Notes: The two J K flip-flops count up. The switches and the logic gates decide when to stop counting and start over.

Design Lab #4

Notes: The universal shift register moves a bit along the outputs. If L1 and L2 are both zero, the next bit shifted in will be a zero.
Design Lab #5

Notes: The universal shift register shifts in a high bit until L3 is lit. When L3 is lit, the register loads in the low bits on inputs A, B, and C. The 4-input NAND gate keeps the circuit going as long as a light is on.

Design Lab #6

Notes: The universal shift register loads in the values of A, B, and C, when SW3 changes. Those bits pass through a logic array that sets Q high on the D-latch if the correct combination is applied. The OR gates keep the latch from changing once it’s set. The two NOT gates in a row provide a time delay. There are also extra AND gates to make sure the numbers are supplied in the correct order.
Notes: The universal shift registers move a high bit along the eight outputs. The D flip-flops allow a change in SW8 to act as a “paddle” to hit the “ball” and send it the other direction. The OR gates in series test the outputs and allow the ball to be put into play only when all outputs are zero. The J K flip-flop toggles S1 and S0 in order to determine the direction the ball travels.