Digital Output Audio Preamp

Prototype Design and Product Specification

Calvin College
Engineering 339/340
May 13, 2005

Senior Design Team #2
Patrick Avoke
Nathan Haveman
Nsimah Okonna
Andrew Wallner
1 Executive Summary

Our project goal was the design of a portable audio interface device for consumer use. Such a product would allow the consumer to connect an analog audio source, like a microphone or a musical instrument, to a digital storage device like a USB hard disk or mp3 player. This functionality would grant the ability to easily create CD-quality digital recordings without a personal computer or expensive professional audio equipment. The product design incorporates a digitally-controlled low noise stereo amplifier and a high-resolution analog-to-digital converter. The created digital audio information could be easily converted to multiple output formats including PCM and MPEG encoding. The digital data could also be delivered directly through an S/PDIF output. More usefully, an integrated USB host supports connection to a variety of mass-storage devices for easy file creation and storage.
Table of contents

1 EXECUTIVE SUMMARY ........................................................................................................... 2

2 INTRODUCTION ................................................................................................................... 5
  2.1 PRODUCT .................................................................................................................... 5
  2.2 TEAM .......................................................................................................................... 5

3 PROJECT OVERVIEW ........................................................................................................... 7

4 DESIGN REQUIREMENTS ...................................................................................................... 8
  4.1 DESIGN OBJECTIVES ................................................................................................. 8
    4.1.1 Accuracy ................................................................................................................ 8
    4.1.2 Versatility .............................................................................................................. 8
    4.1.3 Modularity ............................................................................................................ 8
    4.1.4 Portability .............................................................................................................. 8
  4.2 DESIGN NORMS ............................................................................................................. 8
    4.2.1 Cultural Appropriateness ...................................................................................... 8
    4.2.2 Transparency ........................................................................................................ 9
    4.2.3 Stewardship ......................................................................................................... 9
    4.2.4 Integrity ................................................................................................................ 9
    4.2.5 Justice .................................................................................................................. 10
    4.2.6 Caring .................................................................................................................. 10
    4.2.7 Trust ..................................................................................................................... 10

5 PROJECT SPECIFICATION ..................................................................................................... 11
  5.1 PHYSICAL SPECIFICATIONS ......................................................................................... 11
    5.1.1 Enclosure Construction ....................................................................................... 11
    5.1.2 Environmental Tolerance .................................................................................... 11
    5.1.3 Ecological Considerations ................................................................................. 12
  5.2 ELECTRICAL SPECIFICATIONS ..................................................................................... 12
    5.2.1 Input .................................................................................................................... 12
    5.2.2 Output .................................................................................................................. 14
    5.2.3 Power Supply ........................................................................................................ 15
  5.3 USABILITY ...................................................................................................................... 16
    5.3.1 External Connections ......................................................................................... 16
    5.3.2 User Serviceable Components .......................................................................... 16
    5.3.3 User Controls ....................................................................................................... 16
    5.3.4 Indicators to User ............................................................................................... 17

6 DESIGN DEVELOPMENT ....................................................................................................... 18
  6.1 DESIGN OVERVIEW ....................................................................................................... 18
    6.1.1 Block diagram ..................................................................................................... 19
    6.1.2 Concept Drawing ............................................................................................... 20
  6.2 ANALOG / DIGITAL FRONT END .................................................................................. 20
  6.3 ANALOG FRONT END .................................................................................................... 21
    6.3.1 Selection block .................................................................................................... 21
    6.3.2 Differential amplifiers ....................................................................................... 22
    6.3.3 Headphone output ............................................................................................. 22
  6.4 DIGITAL AUDIO SIGNAL PATH .................................................................................... 23
    6.4.1 Digital signal logic format .................................................................................... 23
    6.4.2 Analog to digital conversion .............................................................................. 24
    6.4.3 Sample rate conversion ..................................................................................... 25
6.4.4 Digital output driver .......................................................................................................................... 26
6.5 USB DATA ................................................................................................................................................. 27
6.5.1 Receiving Data from Analog Circuit .................................................................................................... 27
6.5.2 Storing to a USB Mass Storage Device ............................................................................................... 28
6.6 POWER REGULATION AND DISTRIBUTION .................................................................................. 29
6.6.1 Multiple Voltage Levels ..................................................................................................................... 29
6.6.2 48V block (phantom power) ............................................................................................................... 30
6.7 CONTROL CIRCUITRY .......................................................................................................................... 31
6.7.1 User interface ...................................................................................................................................... 31
6.7.2 Preamp Control .................................................................................................................................. 31
7 ECONOMIC ANALYSIS ............................................................................................................................. 32
7.1 TARGET MARKET .................................................................................................................................... 32
7.2 MARKETING STRATEGY ....................................................................................................................... 33
7.3 PRICING STRATEGY ................................................................................................................................. 33
7.4 PROMOTION AND DISTRIBUTION ...................................................................................................... 33
7.5 FINANCIAL ANALYSIS ............................................................................................................................ 33
8 PROJECT EXECUTION ............................................................................................................................... 34
8.1 TEAM MANAGEMENT ............................................................................................................................. 34
8.1.1 Group Organization ............................................................................................................................ 34
8.2 PROJECT BUDGET .................................................................................................................................. 34
9 PROJECT SOLUTION .................................................................................................................................. 36
9.1 ANALOG FRONT END ............................................................................................................................. 36
9.2 USB .......................................................................................................................................................... 36
9.3 POWER .................................................................................................................................................... 37
10 CONCLUSION .............................................................................................................................................. 38
11 RECOMMENDATIONS ............................................................................................................................. 39
12 ACKNOWLEDGEMENTS ........................................................................................................................... 40
A APPENDIX .................................................................................................................................................. 41
A.1 GROUP PHOTO .......................................................................................................................................... 42
A.2 CALCULATIONS ....................................................................................................................................... 43
A.3 ADC TEST: PCM4202 DC VOLTAGE TO BINARY OUTPUT ...................................................................... 47
A.4 ADFE SCHEMATIC ................................................................................................................................... 48
A.5 ADFE PRINTED CIRCUIT BOARD .......................................................................................................... 50
A.6 PREAMP TO ADC AND HEADPHONE AMP CONNECTION SIMULATION ............................................. 53
A.7 ADFE COMPONENT LIST ....................................................................................................................... 56
A.8 CONTROL LOGIC FOR THE OPERATION OF THE PGA2500 .............................................................. 57
A.9 CONTROL LOGIC PROTOTYPE CIRCUIT ............................................................................................... 61
A.10 ECONOMIC ANALYSIS ........................................................................................................................ 62
A.11 POWER REQUIREMENTS ....................................................................................................................... 63
A.12 48V PHANTOM POWER DESIGN ........................................................................................................ 64
A.12.1 48V DC-DC converter schematic ...................................................................................................... 64
A.12.2 48V DC-DC converter parts list ......................................................................................................... 65
A.13 USB SOURCE CODE ............................................................................................................................... 66
2 Introduction

2.1 Product

Originally developed in 1985, the Universal Serial Bus protocol, or USB, has become the standard for connecting electronic peripherals. USB was designed as a cheap, effective, easy to use interface. Since its creation, it has revolutionized the electronics industry. The introduction of USB has also brought about the popularity of Mass Storage Devices. A mass storage device can be anything from a memory card, to a MP3 player, to an external hard drive. These devices attach to a computer, usually through USB, and allow the user to easily transfer files to and from the device.

Recently, there has also been a maturity in the field of digital audio. Audio circuitry has reached a point in history where any further improvements in quality would be unperceivable to the human ear. This circuitry allows the consumer to create digital audio files that rival the quality previously only available through expensive studio recording equipment.

Our design is a bridge between these two fields. We designed a device using high fidelity audio circuitry to record an audio signal as a digital audio file directly onto a mass storage device using USB connectivity. This would allow a consumer to record studio quality audio from nearly any audio source onto almost any digital medium without the use of expensive studio equipment or a bulky computer.

2.2 Team

This team is made up of four members with concentration in Electrical / Computer Engineering:

1. Patrick Avoke from Ghana, West Africa is interested in automation and controls systems. He currently works as technical support personnel in the engineering department labs and this job involves installing workstations and software deployment. His goals for the next five years would be to gain some working experience in automatic controls and then go on to graduate school to study for Masters of Science in controls systems.
2. Nate Haveman hails from Jenison, Michigan. He is graduating with a degree in Electrical/Computer Engineering with minors in Mathematics and Music. He plans on attending graduate school at the University of Michigan to pursue a Masters degree in Signal Processing. Currently, he is working at Eaton Aerospace. He plans to move to Quito, Ecuador for the summer to design an audio studio for HCJB World Radio.

3. Nsimah Okonna hails from Nigeria, West Africa. She minors in Mathematics and has interest in power systems and communications which she hopes to pursue in graduate school. She has worked with Exxon Mobil Corporation as an electrical technician and a facilities engineering intern. Currently, she works as a grader and lab monitor for Calvin’s Engineering and Mathematics departments.

4. Andrew Wallner, originally from Milwaukee, WI, has ties to its northern neighbor Sheboygan, and to the southern crossroads, Chattanooga, TN. His academic interests include analog and digital electronic hardware, audio signal processing, sound reinforcement and recording. Andrew strives to possess competence in a broad range of technical areas including electrical, mechanical, and systems design, fabrication, and implementation.

A group photo is located in the appendix.
3 Project overview

The objective of our design was to construct a device that will record an analog audio signal onto a digital device. We designed this device to be versatile, accurate, modular, and portable.

The design allows a variety of analog audio sources to be connected to a variety of digital storage devices for maximum flexibility. Our device will accept a line-level input (a CD player, record player, or tape player), an instrument level input (a guitar, keyboard, or bass) or a microphone level input (for vocals or other non-electronic instruments). This allows us to connect nearly any audio source to our device. Our device will also connect to any digital device that operates as a mass storage device. These include flash drives, hard disk drives, and MP3 players.

Our audio device will produce high fidelity audio recordings that rival current studio recording equipment. Our design incorporates low noise circuitry with very accurate signal processing to create audio files previously unavailable to the consumer market.

Our device will be self contained; it will not need any other equipment besides an audio source and a digital destination to operate correctly. Our design will not need the help of a computer or any external audio processing equipment to function correctly.

Our design will be small, robust, and self-powered to allow for easy portability. We want our design to a device that allows the user to be able to travel and record high quality audio in environments that were previously difficult to reach. Our device should put into the consumers hand what was previously only available as a room full of high end audio equipment.
4 DESIGN REQUIREMENTS

4.1 Design Objectives

4.1.1 Accuracy
Our device should improve recording sound quality by incorporating wider audio bandwidth, greater dynamic range, and lower noise than other available, portable, consumer-grade recorders.

4.1.2 Versatility
The device should accept multiple input and output format types and operate seamlessly within a variety of contexts.

4.1.3 Modularity
This would be a stand-alone device that does not need to be connected to a computer or any other digital device for it to be functional.

4.1.4 Portability
This would be a compact device of about roughly the size of a typical MP3 player. It will be battery powered for maximum portability.

4.2 Design Norms
Design norms are critical standards for successful design engineering. This design seeks to exhibit commitment to these, and more fundamentally, to naturally reflect the Christian convictions of the designers. The holistic approach to the engineering process represents the integration of a Reformed theological perspective in the context of a nearly-completed liberal arts education.

4.2.1 Cultural Appropriateness
Such a technologically advanced device comes at a cost. In our present society, there is an unquestioned expansion of gadgets and toys in the consumer market. Our convictions regarding cultural appropriateness make us sensitive to how our design fits in to the mainstream anti-frugal middle-class and
seeks to offer a sensible presentation of legitimate human creativity. This final design addresses specific needs of today's youth culture allowing users to easily operate this device without much of a learning curve associated with the process.

4.2.2 Transparency
Transparency was another key consideration in the design of the digital output audio preamplifier.
Transparency, used here, is defined as “free from guile, candid or open”. Since this design simplifies the digital data storage, there was the need to clearly state the capabilities and limitation of this device to ensure that the potential users understand exactly what they can expect from a functioning digital output audio preamplifier. To further support this design norm, the details of the components used as well as the level of successfulness of this design are clearly stated in this report.

4.2.3 Stewardship
The concept of stewardship as a design norm can easily be applied to many different aspects of the design process. As stewards (or caretakers) of God's creation, designing an electrical device meant taking consideration of the effects which our design would have on the user and the environment. With this in mind, we set out to build an efficient design that is aesthetically and functionally simple to operate. To cut cost, and potentially reduce waste of resources and components, we utilized many existing test devices and apparatus in constructing some of our major parts like the printed circuit board.

4.2.4 Integrity
Integrity; defined here as the “steadfast adherence to strict moral and ethical codes of conduct” is evident in the design of the digital output audio preamplifier. Integrity as a design norm was vital in streamlining our design process to address an existing consumer need for a product that works well. On the moral front, it was important to truthfully state our areas of competency, what we achieved during the course of the project, and give credit to all other parties that helped in anyway towards the success of this design. As far as ethical codes of conduct go, care has been taken to build a design that has the health and safety of users foremost; ahead of all other considerations.
4.2.5 Justice
Including “justice” as one of the necessary norms in putting together this design alludes to fairness as regards to what is right and what is not. Alternative designs that could achieve similar results have been discussed in the Project Proposal and Feasibility Studies document (PPFS) as a gesture of fairness to designers of these other products as well as to the consumers to give an idea of how our design measures up with the other commercially available alternatives.

Technological ability made available without extensive technical background; empowerment. This ability still comes at a price, it is a luxury.

4.2.6 Caring
Care for the needs and health of the consumer has been the primary motivation for a modular, portable, versatile and accurate digital output audio preamplifier. A deeper care for the environment we live in is further motivation for improving our design to meet the needs of the consumer.

4.2.7 Trust
We are establishing a reputation with this device. As budding professionals, we are entrusted with the task of building the best possible design to address the consumers’ needs. Oftentimes, clients state requirements and want to see physical results to prove that the product works well. With the trust imposed on us, we have worked tirelessly to make a device that addresses the requirements of consumers. This saves users the trouble of grappling with the intricate details of data transfer from one point to the other.
5  Project Specification

5.1  Physical Specifications

5.1.1  Enclosure Construction

The enclosure shall be constructed using a combination of the following materials: aluminum, stainless steel, or reinforced thermo-set plastic. If a plastic material is utilized, a metallic material must also be used within or in parallel to it and shall provide RFI shielding equivalent to 99% metallic coverage.

The enclosure shall be assembled using stainless steel screws. The assembly shall be such that disassembly by a trained service person may be conducted without any damage to the enclosure or contained components.

The enclosure shall be impermeable to debris commonly produced and found within the side pockets of common pants.

The enclosure shall provide limited resistance to the entrance of liquid droplets. If a design is implemented wherein the continuous external surface of the enclosure is interrupted by seams or holes for the passage of switches, buttons, connectors, lamps, displays, bezels, gauges, paperclips, toothpicks, batteries, or any object specified to be part of the normal operation of the device, some means shall be provided to inhibit the flow or seepage of liquid into the enclosure. In this case, liquid shall refer to any condensed fluid mixture.

The device should be of similar size and form to a PDA.

5.1.2  Environmental Tolerance

The device shall be able to withstand the impact of falling onto a reinforced concrete floor from a height of 3 meters at least 8 times with no performance degradation.
The device shall be able to withstand the impact of falling onto a reinforced concrete floor from a height of 1 meter at least 100 times with no apparent cosmetic deformation greater than 0.2mm.

The device shall not be damaged while stored within the temperature range from -30°C to 90°C.

The device shall not be damaged while stored within condensing water atmospheres.

The device shall be capable of operation within the temperature range from 0°C to 30°C with no performance degradation.

The device shall be capable of operation within the temperature range from -20°C to 50°C with no performance degradation except reduction in battery life.

The device shall be capable of operation within atmospheres of 5% to 95% RH, non-condensing.

5.1.3 Ecological Considerations

The device shall be constructed with at least 1% recycled material.

The device enclosure shall not have any dissimilar component materials joined in a manner which makes them mechanically inseparable. In this case, heat is considered to be an appropriate catalyst for mechanical separation.

5.2 Electrical Specifications

5.2.1 Input

5.2.1.1 Analog Audio

5.2.1.1.1 Connections

The device shall be capable of using two (2) analog inputs during any time of operation.

The device shall have four (4), three-conductor, differential-voltage, balanced-impedance inputs each with a common reference conductor.

Two (2), three-conductor, differential-voltage, balanced-impedance inputs each with a common reference conductor shall be named “microphone” or “mic” inputs.
The microphone inputs shall each be terminated with non-locking female XLR connectors.

Two (2), three-conductor, differential-voltage, balanced-impedance inputs each with a common reference conductor shall be named “line” inputs.

The line inputs shall each be terminated with non-locking 6.5mm female TRS phone connectors.

One microphone input connector and one line input connector shall be combined in a Neutrik combo connector and shall be further named the LEFT input connector.

One microphone input connector and one line input connector shall be combined in a Neutrik combo connector and shall be further named the RIGHT input connector.

5.2.1.1.2 Microphone Inputs, ratings

Each microphone input shall be capable of receiving signals in the frequency range of 10Hz to 22 kHz. Deviation from linearity in amplitude or phase shall not exceed +/- 0.02 dBu and +/- 2° respectively.

Each microphone input shall have a nominal impedance of 3kΩ.

Each microphone input, set at the minimum gain, shall register a 0dBfs value for a 1 kHz sinusoidal input stimulus of amplitude 5 dBu.

Each microphone input, set at the maximum gain, shall register a 0dBfs value for a 1 kHz sinusoidal input stimulus of amplitude -45 dBu.

5.2.1.1.3 Line Inputs, ratings

Each microphone input shall be capable of receiving signals in the frequency range of 10Hz to 22 kHz. Deviation from linearity in amplitude or phase shall not exceed +/- .05 dBu and +/- 10° respectively.

Each line input shall have a nominal impedance of 150 kΩ.
Each line input, set at the minimum gain, shall register a 0dBfs value for a 1 kHz sinusoidal input stimulus of amplitude 24 dBu.

Each line input, set at the maximum gain, shall register a 0dBfs value for a 1 kHz sinusoidal input stimulus of amplitude of -26 dBu.

5.2.1.2 External Power

5.2.1.2.1 Connections
The device may be capable of receiving external power through a suitable polarized connector with no dimension along the surface of the device enclosure greater than 10mm.

The device may receive external DC power through a USB connector.

5.2.1.2.2 Power input ratings
The external power input shall be designed to receive dc power.

The external power input shall have reverse-polarity protection.

The external power input shall have an internal emergency over-current limiting device.

The external power input shall have RFI noise filtering.

A non-USB external power input shall be rated to provide sufficient power for the device operation and for the simultaneous recharge of the internal battery.

A USB power input shall conform to all USB Implementers Forum, Inc. specifications regarding power consumption from the USB.

5.2.2 Output

5.2.2.1 Digital Audio Output
The digital audio output shall be compatible with the AES-3 format for serial transmission of digital audio.
The digital audio output must conform to the Sony/Philips Digital Interconnect Format (S/PDIF) interface as specified in (IEC-958) and is summarized as follows:

<table>
<thead>
<tr>
<th>Connector</th>
<th>RCA (phono)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal level</td>
<td>0.5 to 1V</td>
</tr>
<tr>
<td>Modulation</td>
<td>biphase-mark-code</td>
</tr>
<tr>
<td>Max. Resolution</td>
<td>24 bit</td>
</tr>
</tbody>
</table>

5.2.2.2 Headphone Output

An output shall be provided for monitoring the analog outputs of the left and right channel input amplifiers. The output shall be named the “headphone” output and must deliver separate signals for the left and right inputs.

The headphone output connector shall be a 3.5 mm TRS phone jack or a 6.5 mm TRS phone jack.

Max output level for 0dBfs audio signal: 3 V rms into 600 ohm load.

5.2.2.3 USB Output

An output shall be provided for connection to a USB mass storage device.

The output shall be intended for the delivery of data to the mass storage and shall also permit bidirectional communication for the purpose of negotiating the intended data transfer.

The output shall conform to all applicable USB Implementers Forum, Inc. specifications.

5.2.3 Power Supply

The device shall provide a regulated and filtered 48 V output for the powering of condenser microphone input circuitry.

The 48V output for the powering of condenser microphone input circuitry shall be called “phantom power.”

The phantom power + 48 V output shall be applied to the XLR microphone input pins 2 and 3.
The phantom power 0 V ground shall be connected to the XLR microphone input pin 1.

Provision shall be made to disconnect the phantom power voltage from the microphone input.

5.3 Usability

5.3.1 External Connections
The location, orientation, and marking of connectors, ports, panels, etc. shall be such that a user familiar with portable electronic devices would not easily confuse an assumed function with a purpose intended by the designer.

5.3.2 User Serviceable Components
The internal rechargeable battery shall be user serviceable.

There shall be no user serviceable electronic components within the device except the rechargeable battery.

5.3.3 User Controls
The user shall be granted the ability to control all of the following items:

- Left channel input gain, in increments of 1dB or smaller
- Right channel input gain, in increments of 1dB or smaller
- Headphone output level in increments of 3dB or smaller
- Output sample rate
- Output word length
- Start/stop recording to USB MSD
- Phantom power present at microphone inputs
- System power on/off
5.3.4 Indicators to User

5.3.4.1 External markings

The device shall provide visual indicators adjacent to each external connector to denote its intended use.

5.3.4.2 System state indicators

The device shall provide illuminated visual indicators to inform the user of the following system parameters:

- Power on
- USB MSD ready
- Recording
- Sample rate
- Sample word length
- Left channel gain
- Right channel gain
- Left input at -40dBfs
- Right input at -40dBfs
- Left output at 0dBfs
- Right output at 0dBfs

The device may provide alternate non-visual indicators for system operation by visually impaired persons. It is recommended that such indicators be tactile and not audible nor rely on olfactory perception.
6 Design Development

6.1 Design overview

We divided our design into 5 major functional blocks: the Preamp, the Analog to Digital Converter (ADC), the Output, the USB, and the Control.

The Preamp block will provide connectivity to a variety of audio sources. It will then amplify the analog audio signal received from these sources to a level sufficient for the ADC block.

The ADC block will receive the analog audio signal from the Preamp block, filter it appropriately, and convert it into a digital signal. It will then verify that the digital signal is formatted correctly and forward it to the Output and USB blocks.

The Output block allows our device to connect with a variety of analog and digital signal devices. This block receives a signal from the ADC block and outputs to either a line level output suitable for headphones or a S/PDIF level output for connection to high end digital audio equipment.

The USB block allows the device to record to other digital devices. It receives the digital signal from the ADC, buffers the data, forms a valid file structure, and stores the file onto a digital device. This stage is quite complicated since the USB block needs to act as a host to the connected digital device, meaning that the USB block needs to command the device how to function correctly.

The Control block controls the operation of our entire device. It provides an interface between the different blocks of the device and the user. It tells the user when there is a valid digital device ready to be recorded to, when the device is receiving an audio signal, and allows the user to make adjustments to the recording process. It also provides appropriate power to each of the blocks.
6.1.1 Block diagram

- MICROPHONE
- ANALOG SIGNAL
- SELECTION
- DIFF. AMPLIFIER
- FILTER
- A/D
- FIFO TFR
- PREAMP
- CONTROL
- 48V
- ADC
- OUTPUT
- IPOD COMM
- HEADPHONE LINE DRIVER
- SPDIF LINE DRIVER
- FIFO BUFFER
- FILE CONTROL
- USB HOST
- HEADPHONES
- CD-R, ETC.
- I-POD
6.2 Analog / Digital Front End
Because of the interdependent nature of the analog and digital signal circuitry, the analog and digital signal functional blocks were developed simultaneously. This subsystem is referred to as the Analog Digital Front End (ADFE) or simply the signal path circuitry. A complete schematic and PCB images of the ADFE circuitry is provided in the Appendix. Unique characteristics of the analog and digital sections are discussed separately in the following sections.
6.3 Analog front end

This block is essential for gain control of the line input or microphone input to the Digital Output Audio Preamplifier. It consists of four smaller blocks namely the: 1) 48V (phantom power) block, 2) input selection block, and 3) differential amplifier block 4) headphone amplifier block. A schematic of the analog components is shown in Figure 6.3.2.

![Analog signal path schematic](image)

Figure 6.3.2. Analog signal path schematic.

6.3.1 Selection block

This is made up of two selectors (for both left and right) that are used in connecting the microphone and line outputs as inputs to the differential amplifier. The line input requires a 6.5mm tip ring sleeve (TRS) phone jack connector while the microphone input requires a female three pin XLR connector. The selection block also incorporates a switch which is used to switch between both inputs.

This requirement would be met by using two combination jacks that have connections for both inputs and also incorporate an internal switch in each.
Suggested product is from Neutrik with model number: NCJ9FI – H – O

6.3.2 Differential amplifiers
This is made up of the preamplifier that is used for gain control. It takes in either the line input or microphone input and amplifies it, depending on the required gain. Gain range is between 0dB to 65dB.
This requirement would be met by using two digitally controlled preamplifiers. Reasons for choosing the digitally controlled preamplifier include:

- It does all its amplification in this single chip.
- Eliminates the time required to put different circuits together.
- Draws less power.
- Reduces space required in placing all the components.
- Does not require additional buffers, decoders or multiplexers.
- Eliminates the cost of the afore mentioned components

Selected product is from Texas instruments with model number: PGA2500.

6.3.3 Headphone output
The headphone output provides gives the user the ability to listen to the audio being delivered to the ADC. The output signal is produced by the headphone amplifier, a single IC, class AB stereo power amplifier. The left and right balanced input signals are ac-coupled to the outputs of the PGA2500 preamplifier ICs. The outputs of the headphone amplifier are delivered to the headphone connector through dc-blocking capacitors. The calculations used to select the capacitance values are listed in the appendix.

The headphone amplifier gain control, like the microphone preamps, is also digital. This feature permitted a simple connection to the user interface through the digital control system. The device selected for use contained logic which permitted independent, asynchronous gain selection. This functionality required only two simple inputs for volume increment up and volume increment down. The amplifier IC contains memory elements that store the selected gain setting. An input is provided for connection to a non-switched battery power source, and a memory maintenance capacitor is provided to
briefly hold the stored value when the battery voltage is removed. The IC selected was a Texas Instruments TPA0252. A similar model was considered, which incorporated serial gain selection, but was not selected because of the added control logic complexity.

6.4 Digital Audio Signal Path
The digital audio signal path originates at the analog to digital converter, progresses through the sample rate converter, and is then delivered simultaneously to the USB subsystem and digital output driver. A section of the ADFE showing the Digital Audio Signal path components is shown in Figure 6.4.

The logic circuitry that the digital signal path is comprised of is based on 3.3 V CMOS technology. Some core voltages of selected components operate at 5 V.

![Figure 6.4 Digital signal path schematic.](image)

6.4.1 Digital signal logic format
Throughout the device, the digitized audio data is conveyed in a three-signal format consisting of a bit-clock, word clock, and serial data line. This arrangement permits straightforward identification of bit-
order and sample frames. The rising edge of the bit clock indicates a valid data bit. The word clock high
indicates the presence of data corresponding to the Left channel and conversely, the word clock low
indicates right channel data. The order of the bits within the data word varies according to the system’s
mode of operation. Three schemes of bit ordering were found to be typical among digital audio
components. They are Left Justified, Right Justified, and I²R and are depicted in Figure 6.4.1

![Figure 6.4.1 PCM Data Formats: Left Justified, Right Justified, and Philips I²S](image)

In each ordering scheme, the data value is transmitted as a twos-complement value with the most-significant bit first. While it is desirable to select only one ordering scheme for implementation within a
particular design, the use of the two justified modes allowed for simplification and increased robustness
of the system design. It should be noted that the use of the widely-accepted I²S format would allow
compatibility with an increased number of integrated circuits from various manufacturers. I²S is a
versatile protocol for “single wire” communication and will be discussed briefly in the context of the
control logic.

### 6.4.2 Analog to digital conversion

Analog to digital conversion takes place within a single integrated circuit. The ADC selected is of the
delta-sigma type. This oversampling method increases the quantization accuracy of each output sample by
reporting a calculated average value for the sample period. This average is computed by sampling the
analog input into more divisions, or deltas, per unit time than required by output rate. The amplitude value measured at each time is scaled by the reciprocal of oversampling rate and the sum, sigma, is accumulated for all of the deltas within the sample period. This process yields two major benefits for the representation of sampled audio signals. First, the sample produced represents a value closer to the true mean value of the time period being measured, which is most significant when capturing transient sounds with frequency components outside of the audible spectrum and when representing the zero-crossings of low frequency tones. Secondly, the oversampling essentially increases the Nyquist rate of the sampling process and tends to function as a digital low-pass filter. The filtering action decreases the aliasing effects of the sampling process, and permits the use of a mere first-order analog anti-aliasing at the ADC input. This reduces the complexity of the required circuitry and potential for the filter non-idealities associated with higher order Bessel, Butterworth, and Chebychev filters. The IC selected was chosen based on its performance characteristics, compatibility with other specified components, vendor preference and the availability of interchangeable or nearly interchangeable components from multiple manufacturers. The ADC operates with 24-bit resolution, that is, it represents the positive input voltage within the reference voltage range on a scale of 0 to 8388608. The reference voltage is 3.0V, so the precision of the ADC is to within +/- 0.4 uV. The ADC operates at an output sample rate of 96 kHz with 64 times oversampling or at 44.1 kHz using 128 times oversampling. The ADC selected was the Texas Instruments PCM4202. Both the TI PCM4202 and PCM1804 were used in prototype development.

### 6.4.3 Sample rate conversion

Sample rate conversion and word length reduction takes place within a single integrated circuit. Sample rate conversion is not strictly necessary to achieve the specified output sample rates because it is possible to configure the ADC in conjunction with a properly selected master clock frequency for the desired output. The sample rate converter does, however, give the design flexibility for future support of additional standard outputs. This foresight is directly in line with the fundamental design goal of versatility.
As implemented in the current design, the sample rate converter’s primary responsibility is to reduce the word length of the ADC output to the appropriate length for the digital outputs. Early in the design process, it became apparent that it would be necessary to use an ADC of higher precision than the specified output resolution. Thus, word length alteration must be addressed. The most straightforward method of shortening word length is to simply truncate the data by disregarding the superfluous bits. In many situations, truncation can be used with acceptable losses of precision and accuracy. In general, for any particular sample, truncation only affects the accuracy of the LSB. When the value of the LSB is misrepresented over a number of samples, the single bit errors can cause phase errors in the accumulated signal with a magnitude on the order of what might be produced by errors in the two least significant bits. A more accurate method of reducing a data word involves averaging the superfluous bits to select an appropriate value for the LSB to be generated. If the sample rate is altered at the same time, undesirable digital filtering can occur. This phenomenon is avoided by interpolating the data to, in a sense, perform calculations at a higher precision before the result is selected. The interpolation, calculation, averaging process is referred to as dithering and is considered the most superior method of word length reduction.

Digital signal theory and esoteric philosophies of representation aside, the most compelling reason for selecting the sample rate converter was that it would provide a mechanism for the asynchronous transfer of digitized data. In a recording situation, it is imperative that the clock for the ADC be as accurate as possible. Digital signals, sampled with an incorrect or inconsistent clock frequency will forever be inaccurate. An asynchronous buffer between the ADC clock and the USB clock allows the data to be produced at a selected precise rate and be delivered at any other rate. The sample rate converter selected was the Texas Instruments SRC4192.

6.4.4 Digital output driver

In this design, the digital output signal is similar to the internal data format, with one noticeable difference being the reversed word bit order. The digital output driver IC is the device which properly rearranges the data into the AES-3 format. The formatting operation includes insertion of indexing and
indicator bits. Finally, this component provides power amplification to drive external circuitry from the internal digital signals. A diagram of the output data format is shown in Figure 6.4.4.

![Figure 6.4.4. AES-3 frame format.](image)

**6.5 USB Data**

Interfacing the digital output audio preamplifiers to a USB mass storage device involved activating two primary functions on the Cypress EZ-Host development board: receiving the digitized output from the preamp Printed Circuit Board (PCB) in the right format into the EZ-Host development board and making the Cypress EZ-Host board recognize the connection of any USB mass storage device, reading from and writing data to that mass storage device.

**6.5.1 Receiving Data from Analog Circuit**

The process of receiving digitized data from the preamplifier largely depended on the input serial data (SDIN) format from the sample rate converter, the word clock and the bit clock. Since we received data from the preamp, the audio port mode for the sample rate converter (SRC4193) was set to master mode hence the word clock (LRCKI) and bit clock (BCKI) were configured as outputs derived from the reference clock input (RCKI) provided by the EZ-Host board.

Below is a graphical representation of the right justified data format that works with the selected sample rate converter (SRC4193):
The EZ-Host development board was configured as a host to receive LRCKI, BCKI and SDIN as inputs. To achieve this task, a C program was written to recognize the right justified data format. With a right justified input format, one had to figure out a clever way to pick only the last sixteen bits after the word clock is triggered high or low making thirty-two bits after every cycle. The bit clock asserts all the necessary bits coming from the serial line.

Another interesting function of the EZ-Host board was the ability to switch the board to Serial Peripheral Interface mode (SPI). The SPI is a three-wire synchronous interface used to access the on chip control registers of the CY7C67300. To receive data from an external device (the preamp), the Cypress EZ-Host board had to be configured in slave mode. SPI allows the user to simply connect a serial data line from any other device pointing to some memory location rather than having to connect each bit to some input or output pin. Since general purpose input and output pins are memory-mapped, pointers were set to get data from the preamplifier to some chosen memory location.

Once all this is configured with the inputs connected, the program is run whilst the preamp is turned on. The idea here is to have the preamp data temporarily stored in memory on the EZ-Host development board after each work clock cycle. This data could then be stored onto a mass storage device.

### 6.5.2 Storing to a USB Mass Storage Device

For a digital device to operate correctly when connected to our device, a few steps are necessary:

1. Our device must recognize the storage device.
When a storage device is connected, our device must acknowledge the connection, determine what type of device is connected, and verify that it is a valid device.

2. Our device must initialize the correct drivers.

   Our device must determine how to correctly communicate with the external device.

3. Our device must recognize the file format of the device.

   Our device must then analyze the data structure of the device and verify that there is space on the device for the file to be stored.

4. Our device must create a new file.

   Our device needs to set aside a portion of the memory from the external device to allow the data to be recorded. It must also update the directory system so that the external device recognizes the file format.

5. Our device must record to the file.

   Our device must correctly store the digital signal into the memory of the external device.

6. Our device must close the file.

   Our device must properly close the file and allow the external device to be removed without damage to any data. It must also add any additional file information that may be necessary to properly access the file in the future.

### 6.6 Power Regulation and Distribution

#### 6.6.1 Multiple Voltage Levels

This design requires multiple voltage sources for proper operation. A table of power requirements is listed in the appendix. All of the voltages and accompanying current demands can be met using regulated battery-power. A unique requirement of this product is its need for a 48 V supply to be developed from a nominal 6 V battery. This need and a design solution is presented in the next section.
6.6.2 48V block (phantom power)

This is the phantom power that is required by the internal electronics of condenser microphones. It is 48V DC power supply in which its positive terminal is connected to both signal leads of a microphone and its negative terminal to the ground connection. This requirement would be met by using a DC to DC voltage regulator to convert our 6V power supply voltage to 48V for this block. The maximum short circuit current for each microphone Input is given as follows:

\[
V_{\text{phantom}} := 48\text{V} \\
R_{\text{balance}} := 610\Omega \\
I_{\text{phantomMAX}} := \frac{V_{\text{phantom}}}{2R_{\text{balance}}} \\
I_{\text{phantomMAX}} = 3.934 \times 10^{-3} \text{A}
\]

The 48V supply can be generated using a filtered, high-frequency DC-DC boost converter. A proposed design is shown in Figure 6.6.2. It is capable of maintaining a 48VDC output at up to 0.04A with an input voltage of 4 to 6 VDC. More information about this design is available in the appendix.

![Figure 6.6.2: 6 to 48V DC-DC boost converter](http://www.national.com/)
6.7 Control Circuitry

The control circuitry directs the operation of all of the functional blocks. The control circuitry translates inputs from the user interface into the signals that affect the operation of the system components. The control circuitry also translates system output signals into a format meaningful to the user.

6.7.1 User interface

The user interface consists of parameter selection controls and parameter value controls. The user selects which parameter to alter with the former and chooses a desired value with the latter. In such an arrangement, only one parameter may be modified at a time.

6.7.2 Preamp Control

The PGA2500 microphone preamplifier ICs receive gain instruction through a serially-entered 16 bit word. This word is generated based on the user input received through the gain control push buttons. This functionality was successfully demonstrated in the prototype. The hardware used to implement the functionality was a programmable logic device. The programmable logic allowed modifications to be made in the circuit behavior without manual reconfiguration of the components. An extremely valuable feature incorporated into the prototype design was a JTAG port. The JTAG connection allowed almost instantaneous reprogramming of the logic device. The logic device selected was a very economical member of the Altera MAX family, the EPM3064ALC-10. The logic description and circuit arrangement are provided in the appendix.
7 ECONOMIC ANALYSIS

This analysis is carried out to estimate the revenue that could be realized from the sales of the Digital Output Audio Preamp if it were mass produced. This is done under the assumption that this is a new product of an already existing company.

7.1 Target Market

This is the market in which we are planning to sell this product. The people include musicians, music enthusiasts, and students. This target market includes people of various income levels, gender, marital status, age, education, and lifestyle. This product is mainly produced for the American market, although it may be used globally.

We are specifically targeting the Apple I-Pod market although the market is larger for this product. The Apple I-Pod market holds about 90% of the global market for portable MP3 players. According to Phil Schiller, Apple’s vice president of worldwide marketing, “It’s (I-Pod sales) just hitting all demographics – all age groups. It’s really exciting people’s idea of music again, and made people fall back in love with music.” Apple has sold over 15 million I-Pods to date with over 5 million sold in the first 3 months of 2005. Apple predicts that sales will continue to rise with over 23.5 million expected to sell by 2006 and over 100 million by 2008. The I-Pod Shuffle and I-Pod Photo have also been added to the MP3 market by Apple to specifically target the Low and High end markets respectively. The digital music market has also been on the rise with over 200 million digital music tracks downloaded legally and many more illegally.

The market for recording digital music has also been on the rise. The release of amateur recording software, like Apple’s GarageBand or Sony’s Acid, indicates a surge in personal home recording. Assuming 1 million people buy our device during the first year and assuming a 25% increase yearly increase in sales, at the end of five years, approximately 3 million devices would have been sold.
7.2 Marketing Strategy
After accessing the target market, the next step is to develop a strategy on how to market this product. Awareness of the product and its value needs to be created by communicating product information to the target market by way of advertising through internet, billboards, circulating flyers, etc. Also, this can be accomplished through personal selling, sales promotions, and public relations.

7.3 Pricing Strategy
This product is estimated to be sold at an initial cost of $200. $200 is the average cost of parts for building one DOAP. With time, the price will decrease due to aging technology and also discounts and sales that would be offered.

7.4 Promotion and Distribution
Discounts and sales promotion will be offered in order to attract customers and also to provide information about the product. This will aid the customers to make intelligent decisions on how the product meets their needs. The product could be sold online, in electronic stores like Best Buy, Circuit City, and also in retail stores.

7.5 Financial Analysis
See appendix for an income statement from the sales of this product over an estimated period of five years. The cost of items per part is estimated at $60. It is estimated that the cost of rework would be about $30 and that about an average of 15% of total quantity produced could be rework. The manufacturing cost of a two layer board which was used in the production of the prototype is estimated at $3. The return on investment is estimated to be about 27% which is high. Hence the full-scale production of the DOAP would be a worthwhile and profitable business.
8 PROJECT EXECUTION

8.1 Team Management
Needless to say, team management has been rather challenging especially in the area of working around each others schedule to get things done. Although we had a descriptive schedule at the beginning of the project, we quickly observed that we were lagging behind on scheduled tasks ostensibly as a result of an unanticipated extension in the period for research into USB interfacing and other components of the board.

For this project, tasks were divided amongst all four members of the team based on the main functional parts of the design. Major functional parts of this project included the design of the preamplifier as well as corresponding control circuitry and also the interfacing preamplifier with USB.

8.1.1 Group Organization
As it turns out, weekly status reports that elucidate individual hours worked, tasks and accomplishments for that week and team meetings that allowed for updates on progress for each section we were responsible for were very helpful in keeping each other up to speed on general progress of the entire project as well as what each person had to do to get the project done.

8.2 Project Budget
An estimate for the project expenses was developed and presented in the Project Proposal and Feasibility Study. This budget identified expenses expected to total $600. The budget was approved for the execution of this project. The expenses actually incurred during the project were all funded by the original cost estimate. However, the breakdown of the expenses was somewhat different. The project expenses are listed in Table 8.2.
### Table 8.2 Project Expenses

**Team 2 Project Expenses**

<table>
<thead>
<tr>
<th></th>
<th>Estimated Expenses</th>
<th>Actual Expenses</th>
</tr>
</thead>
<tbody>
<tr>
<td>development materials</td>
<td>$200</td>
<td>$80</td>
</tr>
<tr>
<td>components</td>
<td>$250</td>
<td>$320</td>
</tr>
<tr>
<td>publishing</td>
<td>$150</td>
<td>$60</td>
</tr>
<tr>
<td>software</td>
<td>$140</td>
<td>$140</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>$600</strong></td>
<td><strong>$600</strong></td>
</tr>
</tbody>
</table>

#### Estimated Expenses

- Development materials: 33%
- Components: 25%
- Publishing: 42%
- Software: 10%

#### Actual Expenses

- Development materials: 23%
- Components: 54%
- Publishing: 13%
- Software: 10%

![Pie chart showing estimated and actual expenses](chart.png)
9 PROJECT SOLUTION

9.1 Analog front end

The analog front end circuit was laid out on a printed circuit board which was manufactured and produced in-house using Calvin College’s equipment in the electronics laboratory. The printed circuit board housed most of the major components of the design in a bit to emphasis prototype portability. This circuit can take in both microphone and line inputs. It also has both headphone and digital outputs, thereby displaying versatility.

48V block

This voltage is required when condenser microphones are connected to the prototype. Resistors were incorporated in the design for use when condenser microphones are connected to the device.

Selection block

Two combination selectors which were suggested for use in the design were purchased and incorporated in the device.

Differential amplifier

Two digitally controlled preamplifiers were purchased from Texas instruments and incorporated in to the prototype for gain control. The gain can be adjusted from 0dB to 65dB in increments of 1dB. The outputs of the preamplifiers are sent to the analog to digital converter, where the conversion from analog to digital audio signals takes place. Problems were encountered in a bit to control the preamplifiers. These were finally solved with the use of a control circuit which incorporated a field programmable logic array chip (FPGA) to control its operation.

9.2 USB

To perform the functionality desired of our USB block, we used the Cypress EZ-Host development board which utilizes the Cypress CY7C67300 USB controller processor. When we started this project, there
were only a few processors designed specifically to operate as a USB controller. Of these controllers, the Cypress processor provided the most functionality for our design. With this board, we wrote code to implement the steps described in section 4.X. The code was written using the C programming language. It allowed the controller to perform the required tasks without the help of external commands. A description of the files used to perform these tasks may be found in Appendix X. Unfortunately, we experienced a major power failure on our development board and were unable to create a working prototype. We do, however, have verification that our code was operating correctly and provided the functionality which we desired.

The successfully developed program would interface the preamplifier and EZHost board to acquire 32 bit data word from the serial data line input (16 bits for left and right clocks respectively) for every complete word clock (LRCKI) cycle. This program utilized the serial peripheral interface (SPI) configuration of the EZHost board that allowed the board to be modeled as an SPI slave device controlled by steaming data input from the preamplifier and temporarily stores the data in some memory location for transport to the USB mass storage device.

For this part of the process, I could only test the functionality of the program theoretically by running the program to see whether it actually does compile. Full testing was not possible at the time because the EZhost development board got damaged as a result of some power problems encountered on the board.

### 9.3 Power

For the final prototype, power supplies were used in providing power at the level required by the different components. The power supplies were connected to the prototype with the aid of wire connectors.
10 Conclusion

Through our prototyping and simulations, we have proven that our design functions correctly. We have successfully designed a device to record an analog audio signal onto a digital medium. We have achieved our goals of creating a design that is versatile, accurate, modular, and portable. From our analysis, we believe that our device would have a potential place in industry if it were manufactured.

To conclude, we are deeply satisfied with the progress of this project from concept stage through design and building process. Although there are a few other areas that could have been fine-tuned, we are confident that with the constraint of our budget and available time, we have achieved the goals of our project and more importantly have learnt a great deal about teamwork, delegation, scheduling and other existing factors that are always present in any real engineering design environment.
11 Recommendations

Recently, Cypress Semiconductors has released a development kit specifically targeted towards developers interfacing with mass storage devices. The development kit is part number CY4640. I would recommend that any team seeking to do a similar project in the future should research this board and look into using it for their prototyping. Cypress provides a lot of documentation and has excellent customer support. I would definitely recommend working with them.

In the course of this project, as would be expected, we encountered a couple of challenges. First, the project scope was very wide, especially with the USB implementation which we had no experience with and could not even get help or advise from any one until we finally got in touch with a USB consultant by name John Hyde. If we were to redo the project, we would limit the scope in order to do a much more thorough job.

The success of any project that requires the integration of different sections (eg. hardware and software parts of a design) hinges heavily on one’s ability to accurately communicate the structure and function of expected input, output and control signals amongst all persons involved. This especially proved crucial during the preamplifier-EZhost interface portions of the project.

Generally it is always a good idea to try getting all components of the design onto a single printed circuit board (if at all possible) particularly for designs in which timing details, noise and bit losses are critical for success.

Always check and recheck each major component critical for the success of the design and make sure that it does what it should far in advance.

Always prepare for the unexpected and make contingency plans accordingly.
12 Acknowledgements

We would love to extend our sincere gratitude to the following persons as well as everyone who contributed tremendously to the success of this project.

Bassil El-Kadi – Cypress representative

Bill Parlin – Crimp Circuits company

Chuck Holwerda – Calvin College electronic shop

Jody Milewski - Cypress representative

John Hyde – USB consultant

Robert Dekraker – Calvin College Engineering department

Robert Medema – Professor, Calvin College Business department

Steven Vanderleest – Team advisor and Professor, Calvin College Engineering department

Tim Thierault – Industrial consultant

Carl Hordyk – Calvin College Technical Services

Needless to say, we are grateful to God Almighty for good health, wisdom, patience and the ability to bring what was just a fusion of ideas into what we have accomplished hitherto. Again many thanks and God Bless.
A Appendix

Contents

A.1 GROUP PHOTO 42
A.2 CALCULATIONS 43
A.3 ADC TEST: PCM4202 DC VOLTAGE TO BINARY OUTPUT 47
A.4 ADFE SCHEMATIC 48
A.5 ADFE PRINTED CIRCUIT BOARD 50
A.6 PREAMP TO ADC AND HEADPHONE AMP CONNECTION SIMULATION 53
A.7 ADFE COMPONENT LIST 56
A.8 CONTROL LOGIC FOR THE OPERATION OF THE PGA2500 57
A.9 CONTROL LOGIC PROTOTYPE CIRCUIT 61
A.10 ECONOMIC ANALYSIS 62
A.11 POWER REQUIREMENTS 63
A.12 48V PHANTOM POWER DESIGN 64
  A.12.1 48V DC-DC converter schematic 64
  A.12.2 48V DC-DC converter parts list 65
A.13 USB SOURCE CODE 66
Group Photo

Nathan Haveman  Patrick Avoke  Nsimah Okonna  Andrew Wallner
Calculations

**AFE 0dBFS signal levels**

<table>
<thead>
<tr>
<th>PGA2500 specs</th>
<th>PCM4202 specs</th>
</tr>
</thead>
<tbody>
<tr>
<td>$K_{\text{min}} := 10\text{dB}$</td>
<td>$V_{\text{in42FS}} := 3.0\text{V}$</td>
</tr>
<tr>
<td>$K_{\text{max}} := 60\text{dB}$</td>
<td>$\text{dBuV}<em>{\text{42inFS}} := 20\log\left(\frac{V</em>{\text{in42FS}}}{.775\text{V}}\right) = 11.76\text{dBu}$</td>
</tr>
<tr>
<td>$V_{\text{Omax}} := 4.1\text{V}$</td>
<td>$\text{dBuV}<em>{\text{Omax}} := 20\log\left(\frac{V</em>{\text{Omax}}}{.775\text{V}}\right) = 14.47\text{dBu}$</td>
</tr>
</tbody>
</table>

NOTE: (Z.Id = 600 ohm)

required attenuation between PGA2500 and PCM4202 -->

$$\text{dBuV}_{\text{Omax}} - \text{dBuV}_{\text{42inFS}} = 2.71\text{dB}$$

required attenuation between PGA2500 and PCM1804 -->

$$\text{dBuV}_{\text{Omax}} - \text{dBuV}_{\text{18inFS}} = 4.3\text{dB}$$

sensitivity (PGA input to produce 0FS) -->

$$S_{\text{min}} := \text{dBuV}_{\text{Omax}} - K_{\text{min}} \quad S_{\text{min}} = 4.47\text{dBu}$$

$$S_{\text{max}} := \text{dBuV}_{\text{Omax}} - K_{\text{max}} \quad S_{\text{max}} = -45.53\text{dBu}$$

Desired input specs

LINE in sensitivity

$$S_{\text{line min}} := 24\text{dBu}$$

required atten betwn LINE and PGA2500 -->

$$\text{Att}_{\text{line}} := S_{\text{line min}} - S_{\text{min}} \quad \text{Att}_{\text{line}} = 19.53\text{dB}$$

$$S_{\text{line max}} := S_{\text{max}} + \text{Att}_{\text{line}} \quad S_{\text{line max}} = -26$$
**PGA2500 line input attenuator**

Zmic $\Rightarrow$ Zline $\Rightarrow$ Rphnmt $\Rightarrow$ PGAZn/2

$Rpad \Rightarrow C_{block} = 47\mu F$

$CHOOSE \ Rpad \Rightarrow 80.6k$

(should be close to Z.block) divide R1 for balanced input !! (should be close to R.phntm)

$R2 = 186.15$ $R1 = 162k$

$Z1 \Rightarrow 16.5k$ $Z2 \Rightarrow 6.8k + 20$

$K = 10$ $K = 10$

$dB_{att} = 20$ $dB_{att} = 20$

$R3 := 2\sqrt{Z1 \cdot Z2 \left(\frac{K}{K^2 - 1}\right)}$

$R1 := Z1 \cdot \left(\frac{K^2 + 1}{K^2 - 1}\right) - R3$

$R2 := Z2 \cdot \left(\frac{K^2 + 1}{K^2 - 1}\right) - R3$

$R3 = 6.78 \times 10^3$

(should be close to R.phntm)

CHOSE R1 for balanced input !! (should be close to Z.block)

**PCM1804 and TPA0252 input filters**

$PGA2500$ $\Rightarrow$ $ADC$ attenuation / anti alias $\Rightarrow$ $PCM 1804$

$PGA2500$ $\Rightarrow$ $Zsde$ $20k$

$PGA2050$ $\Rightarrow$ $ADC$ attenuation / anti alias $\Rightarrow$ $PCM 1804$

$PGA2500$ $\Rightarrow$ $Rsrc$ $50$

$R9 1000MGE$ $\Rightarrow$ $1uF$

$C1$ $1uF$ $\Rightarrow$ $V+$

$1uF$ $\Rightarrow$ $V-$

$1uF$ $\Rightarrow$ $V+$

$1uF$ $\Rightarrow$ $V-$

$1uF$ $\Rightarrow$ $V+$

$1uF$ $\Rightarrow$ $V-$

$1uF$ $\Rightarrow$ $V+$

$1uF$ $\Rightarrow$ $Zsde$ $20k$

$V+$ $\Rightarrow$ $Zsde$ $20k$

$V+$ $\Rightarrow$ $Zsde$ $20k$

$V+$ $\Rightarrow$ $Zsde$ $20k$

$V+$ $\Rightarrow$ $Zsde$ $20k$

$V+$ $\Rightarrow$ $Zsde$ $20k$
**headphone amp input coupling and impedance buffer**

Amp single-ended input impedance --> \( Z_{hp\text{pin}} := 7k \)

\[
C_{hp\text{inc}} := 1 \cdot 10^{-6} \quad Z_{hp\text{pin}} := \frac{1}{1 \cdot 2\pi \cdot 20 \cdot C_{hp\text{inc}}} \quad Z_{hp\text{Clow}} = 7.96 \times 10^3
\]

\[
f_{hp\text{inc}} := \frac{1}{2\pi \cdot Z_{hp\text{pin}} \cdot C_{hp\text{inc}}} \quad f_{hp\text{inc}} = 22.74
\]

\[Z_{eqHPA} := 2(Z_{hp\text{Clow}} + Z_{hp\text{pin}} + Z_{hp\text{series}}) \quad Z_{eqHPA} = 38.52 \times 10^3
\]

**PCM 1804 attenuator**

\[
\frac{\text{dBpad}}{\text{dBpad}} := 3.86 
\quad K_{pad} := 10^{20} \quad |1 - K_{pad}| = 559.55 \times 10^{-3} 
\quad Z_{thTGT} := 5.4k\Omega 
\quad Z_{ADC\text{ser}} := 4.3k\Omega
\]

\[
K_{iterate} := \frac{Z_{thTGT}}{Z_{ADC\text{ser}} + Z_{thTGT}} \quad K_{iterate} = 556.7 \times 10^{-3}
\]

**PCM 1804 input coupling**

\[
Z_{ADC\text{in}} := 20k\Omega \quad C_{ADC\text{inc}} := 1 \cdot 10^{-6} \quad Z_{shunt} := 51k\Omega
\]

\[
Z_{thADC\text{in}} := \frac{1}{Z_{ADC\text{in}}} + \frac{1}{Z_{shunt}} + \frac{1}{2(Z_{ADC\text{ser}} + 20\Omega)} \quad Z_{thADC\text{in}} = 5.4 \times 10^3 \Omega
\]

\[
f_{ADC\text{in}} := \frac{1}{2\pi \cdot Z_{thADC\text{in}} \cdot 2C_{ADC\text{inc}}} \quad f_{ADC\text{in}} = 14.75\frac{\text{Hz}}{\text{V}}
\]

**PCM 1804 anti-alias filter**

\[
C_{alias} := 1.310^{-9} \quad f_{alias} := \frac{1}{2\pi \cdot Z_{thADC\text{in}} \cdot C_{alias}} \quad f_{alias} = 22.69 \times 10^3 \frac{\text{Hz}}{\text{V}}
\]
passive "T" attenuator

\[ Z_1 := 29k \quad Z_2 := 20k \quad dB_{att} := 24.0 \]

\[ K := 10^{20} \quad K = 15.85 \]

\[ R_3 := 2 \sqrt{Z_1 \cdot Z_2} \left( \frac{K}{K^2 - 1} \right) \quad R_1 := Z_1 \cdot \left( \frac{K^2 + 1}{K^2 - 1} \right) - R_3 \quad R_2 := Z_2 \cdot \left( \frac{K^2 + 1}{K^2 - 1} \right) - R_3 \]

\[ R_3 = 3.05 \times 10^3 \quad R_1 = 26.18 \times 10^3 \quad R_2 = 17.11 \times 10^3 \]

\[ dB_u = \frac{V}{.775V} \]

**Vrms to dBu**

\[ V_{rms} \left( 20 \log \frac{\sqrt{2}}{.775} \right) = 8.75 \]

**dBu to Vrms**

\[ dB_u := 10 \]

\[ \frac{dB_u}{10^{20}} = 2.24 \]

\[ V_{rms} \]

\[ \frac{dB_u}{10^{20}} = 3.16 \]

**Vpp to Vrms**

\[ V_{pp} := 6.2 \]

\[ \frac{V_{pp}}{2 \cdot \sqrt{2}} = 2.19 \]

**Vrms to Vpp**

\[ V_{rms} := 2.2 \]
# ADC test: PCM4202 dc voltage to binary output

## Equipment:
- Fluke 1900A multi-counter
- Wavetek model 190 20MHz function generator
- Tektronix TDS 3032 two channel aw some oscilloscope
- (3 x) HP E3211A DC power supplies
- Agilent E3620A dual output DC power supply

## Settings:
- 11.291MHz
- 11.3MHz
- 3.3, 5.0, 5.0 V

## Vin (dcV) vs. 24..16[dec]

<table>
<thead>
<tr>
<th>Vin (dcV)</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>[24..16]dec</th>
</tr>
</thead>
<tbody>
<tr>
<td>-0.001</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>511</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.00</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.40</td>
</tr>
<tr>
<td>0.01</td>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td>0.60</td>
</tr>
<tr>
<td>0.02</td>
<td></td>
<td>1</td>
<td>1</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.70</td>
</tr>
<tr>
<td>0.03</td>
<td></td>
<td>1</td>
<td>1</td>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.80</td>
</tr>
<tr>
<td>0.04</td>
<td></td>
<td>1</td>
<td>1</td>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.90</td>
</tr>
<tr>
<td>0.05</td>
<td></td>
<td>1</td>
<td>1</td>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.00</td>
</tr>
<tr>
<td>0.06</td>
<td></td>
<td>1</td>
<td>1</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.10</td>
</tr>
<tr>
<td>0.07</td>
<td></td>
<td>1</td>
<td>1</td>
<td>6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.20</td>
</tr>
<tr>
<td>0.08</td>
<td></td>
<td>1</td>
<td>1</td>
<td>7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.30</td>
</tr>
<tr>
<td>0.09</td>
<td></td>
<td>1</td>
<td>1</td>
<td>6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.40</td>
</tr>
<tr>
<td>0.10</td>
<td></td>
<td>1</td>
<td>1</td>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.50</td>
</tr>
<tr>
<td>0.11</td>
<td></td>
<td>1</td>
<td>1</td>
<td>9</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.60</td>
</tr>
<tr>
<td>0.12</td>
<td></td>
<td>1</td>
<td>1</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.70</td>
</tr>
<tr>
<td>0.13</td>
<td></td>
<td>1</td>
<td>1</td>
<td>11</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.80</td>
</tr>
<tr>
<td>0.14</td>
<td></td>
<td>1</td>
<td>1</td>
<td>11</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.90</td>
</tr>
<tr>
<td>0.15</td>
<td></td>
<td>1</td>
<td>1</td>
<td>13</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2.00</td>
</tr>
<tr>
<td>0.16</td>
<td></td>
<td>1</td>
<td>1</td>
<td>13</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2.10</td>
</tr>
<tr>
<td>0.17</td>
<td></td>
<td>1</td>
<td>1</td>
<td>11</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2.20</td>
</tr>
<tr>
<td>0.18</td>
<td></td>
<td>1</td>
<td>1</td>
<td>11</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2.30</td>
</tr>
<tr>
<td>0.19</td>
<td></td>
<td>1</td>
<td>1</td>
<td>16</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2.40</td>
</tr>
<tr>
<td>0.20</td>
<td></td>
<td>1</td>
<td>1</td>
<td>17</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2.50</td>
</tr>
<tr>
<td>0.21</td>
<td></td>
<td>1</td>
<td>1</td>
<td>18</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2.60</td>
</tr>
<tr>
<td>0.22</td>
<td></td>
<td>1</td>
<td>1</td>
<td>19</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2.70</td>
</tr>
<tr>
<td>0.23</td>
<td></td>
<td>1</td>
<td>1</td>
<td>19</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2.80</td>
</tr>
<tr>
<td>0.24</td>
<td></td>
<td>1</td>
<td>1</td>
<td>19</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2.90</td>
</tr>
<tr>
<td>0.25</td>
<td></td>
<td>1</td>
<td>1</td>
<td>20</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.00</td>
</tr>
<tr>
<td>0.26</td>
<td></td>
<td>1</td>
<td>1</td>
<td>21</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.01</td>
</tr>
<tr>
<td>0.27</td>
<td></td>
<td>1</td>
<td>1</td>
<td>22</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.02</td>
</tr>
<tr>
<td>0.28</td>
<td></td>
<td>1</td>
<td>1</td>
<td>23</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.03</td>
</tr>
<tr>
<td>0.29</td>
<td></td>
<td>1</td>
<td>1</td>
<td>24</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.04</td>
</tr>
<tr>
<td>0.30</td>
<td></td>
<td>1</td>
<td>1</td>
<td>25</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.05</td>
</tr>
</tbody>
</table>

## VINL+ & VINL- damaged by +5V input

## Notes:
- Bit 15 was not always measured
- BIT 24 is a sign bit!

## Figure:
- Trace 1 is LRCK=low =VinR
- Trace 2 is DATA
ADFE schematic
ADFE printed circuit board
Preamp to ADC and headphone amp connection simulation

Schematic showing one channel operating at preamp maximum output voltage.

Frequency response of ADC input voltage.
The following two images are screen shots of the ADC input voltage. The values in the cursor windows indicate the expected -3dB frequencies.
Frequency response of ADC input voltage (as above) and headphone amp input voltage. Notice slightly higher signal going to ADC and no LPF (anti-alias) on headphone input.

Screen shot of above plot.
<table>
<thead>
<tr>
<th>Package</th>
<th>Component</th>
<th>Manufacturer</th>
<th>Value</th>
<th>Mfr No.</th>
<th>Vendor No.</th>
<th>Description</th>
<th>Qty/brd</th>
<th>Unit Price</th>
<th>Brd Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>C0805K</td>
<td>C0805C102J5GACTU</td>
<td>Kemet</td>
<td>C0805C102J5GACTU</td>
<td>399-1136-1-ND</td>
<td>Cap, Ceramic COG/NPO, SM, 1000pF ±5%, 500V, 0805</td>
<td>6</td>
<td>0.132</td>
<td>0.792</td>
<td></td>
</tr>
<tr>
<td>PANA F</td>
<td>E6V-FK13470P</td>
<td>Panasonic - ECG</td>
<td>E6V-FK13470P</td>
<td>PCE-3482C-1-TND</td>
<td>Capacitor, Aluminum electrolytic, SM, 47µF ±20%, 630V</td>
<td>4</td>
<td>0.756</td>
<td>3.024</td>
<td></td>
</tr>
<tr>
<td>C0805K</td>
<td>C0805C104K5RACTU</td>
<td>Kemet</td>
<td>C0805C104K5RACTU</td>
<td>399-1170-1-ND</td>
<td>Capacitor, Ceramic X7R, SM, 1µF ±30%, 500V, 0805</td>
<td>22</td>
<td>0.083</td>
<td>1.826</td>
<td></td>
</tr>
<tr>
<td>C0805K</td>
<td>C0805C105K4RACTU</td>
<td>Kemet</td>
<td>C0805C105K4RACTU</td>
<td>399-1284-1-ND</td>
<td>CAP 1.0UF 16V CERAMIC X7R 0805</td>
<td>4</td>
<td>0.182</td>
<td>0.728</td>
<td></td>
</tr>
<tr>
<td>1A3216/18R</td>
<td>C0805C107J5GACTU</td>
<td>Kemet</td>
<td>C0805C107J5GACTU</td>
<td>399-1373-1-ND</td>
<td>Capacitor, Ceramic X7R, SM, 7µF ±30%, 500V, 0805</td>
<td>12</td>
<td>0.175</td>
<td>4.305</td>
<td></td>
</tr>
<tr>
<td>B/3528/21R</td>
<td>C0805C109K4RACTU</td>
<td>Kemet</td>
<td>C0805C109K4RACTU</td>
<td>399-1477-1-ND</td>
<td>Capacitor, Ceramic X7R, SM, 9µF ±30%, 500V, 0805</td>
<td>10</td>
<td>0.189</td>
<td>3.623</td>
<td></td>
</tr>
<tr>
<td>1206</td>
<td>C0805C110K4RACTU</td>
<td>Kemet</td>
<td>C0805C110K4RACTU</td>
<td>399-1577-1-ND</td>
<td>Capacitor, Ceramic X7R, SM, 10µF ±30%, 500V, 0805</td>
<td>10</td>
<td>0.200</td>
<td>4.000</td>
<td></td>
</tr>
<tr>
<td>1206</td>
<td>C0805C111K4RACTU</td>
<td>Kemet</td>
<td>C0805C111K4RACTU</td>
<td>399-1677-1-ND</td>
<td>Capacitor, Ceramic X7R, SM, 11µF ±30%, 500V, 0805</td>
<td>10</td>
<td>0.211</td>
<td>4.220</td>
<td></td>
</tr>
<tr>
<td>1206</td>
<td>C0805C112K5RACTU</td>
<td>Kemet</td>
<td>C0805C112K5RACTU</td>
<td>399-1777-1-ND</td>
<td>Capacitor, Ceramic X7R, SM, 12µF ±30%, 500V, 0805</td>
<td>10</td>
<td>0.222</td>
<td>4.440</td>
<td></td>
</tr>
<tr>
<td>1206</td>
<td>C0805C113K4RACTU</td>
<td>Kemet</td>
<td>C0805C113K4RACTU</td>
<td>399-1877-1-ND</td>
<td>Capacitor, Ceramic X7R, SM, 13µF ±30%, 500V, 0805</td>
<td>10</td>
<td>0.233</td>
<td>4.660</td>
<td></td>
</tr>
<tr>
<td>1206</td>
<td>C0805C114K4RACTU</td>
<td>Kemet</td>
<td>C0805C114K4RACTU</td>
<td>399-1977-1-ND</td>
<td>Capacitor, Ceramic X7R, SM, 14µF ±30%, 500V, 0805</td>
<td>10</td>
<td>0.244</td>
<td>4.880</td>
<td></td>
</tr>
</tbody>
</table>

**Total -> $ 120.85**
Control Logic for the Operation of the PGA2500

LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_unsigned.all;
USE IEEE.std_logic_arith.all;
USE work.sig_types.all;

ENTITY pgatxt IS
  PORT
  ( pb_up       : IN STD_LOGIC;
    pb_dn       : IN STD_LOGIC;
    reset       : IN std_logic;
    clk         : IN STD_LOGIC;
    sw_d1       : IN STD_LOGIC;
    sw_RnL      : IN STD_LOGIC;
    pb_gainzero : IN STD_LOGIC;
    pga_sdo     : OUT STD_LOGIC;
    pga_cs      : OUT STD_LOGIC;
    pga_sdr     : OUT STD_LOGIC;
    pga_sclk    : OUT STD_LOGIC;
    disp_gain   : OUT STD_LOGIC_VECTOR(5 downto 0)
  );
END pgatxt;

ARCHITECTURE pgatxt_architecture OF pgatxt IS
  TYPE STATE_TYPE IS (s0_chkpbs, s1_sendcmd);
  SIGNAL currentState, nextState : STATE_TYPE := s0_chkpbs;
  signal bit_index              : std_logic_vector(4 downto 0) := "11111";
  signal gainL, gainR           : pgagain;
  signal cmdvec                 : STD_LOGIC_VECTOR(31 DOWNTO 0);
  SIGNAL db_pb_up                : STD_LOGIC;
  SIGNAL db_pb_dn                : STD_LOGIC;
  SIGNAL db_up_cnt              : STD_LOGIC_VECTOR (8 DOWNTO 0);
  SIGNAL db_dn_cnt              : STD_LOGIC_VECTOR (8 DOWNTO 0);
BEGIN
pga_sclk <= clk;

PROCESS (clk) -- debounce pb_up using tick counter
BEGIN
  IF pb_up = '1' THEN
    db_up_cnt <= "000000000";
  ELSIF (clk'EVENT AND Clk = '1') THEN
    IF (db_up_cnt /= "111111111") THEN
      db_up_cnt <= db_up_cnt + 1;
    END IF;
  END IF;
  IF (db_up_cnt = "100000000") AND (pb_up = '0') THEN
    db_pb_up <= '0';
  ELSE db_pb_up <= '1';
  END IF;
END PROCESS;

PROCESS (clk) -- debounce pb_dn using tick counter
BEGIN
  IF pb_dn = '1' THEN
    db_dn_cnt <= "000000000";
  ELSIF (clk'EVENT AND Clk = '1') THEN
    IF (db_dn_cnt /= "111111111") THEN
      db_dn_cnt <= db_dn_cnt + 1;
    END IF;
  END IF;
  IF (db_dn_cnt = "100000000") AND (pb_dn = '0') THEN
    db_pb_dn <= '0';
  ELSE db_pb_dn <= '1';
  END IF;
END PROCESS;

PROCESS (clk, reset) -- state machine synchro logic
BEGIN
  IF (reset = '0') then
    bit_index <= "11111";
    gainL <= 0;
    gainR <= 0;
    currentState <= s0_chkpbs:
END PROCESS;

cmdvec <= "010100000000000001010000000000";

elsif (clk'EVENT AND clk = '0') THEN
  currentState <= nextState;
  case currentState is
    when s0_chkpse => -- wait for inputs
      if sw_RnL = '1' then --RIGHT
        disp_gain <= cmdvec(21 downto 16);
        if pb_gainzero = '0' then
          gainR <= 0;
        elsif db_pb_up = '0' then
          gainR <= gainR + 1;
        elsif db_pb_dn = '0' then
          gainR <= gainR - 1;
        elsif sw_d1 /= cmdvec(24) then
          cmdvec(24) <= sw_d1;
        end if;
      else --LEFT
        disp_gain <= cmdvec(5 downto 0);
        if pb_gainzero = '0' then
          gainL <= 0;
        elsif db_pb_up = '0' then
          gainL <= gainL + 1;
        elsif db_pb_dn = '0' then
          gainL <= gainL - 1;
        elsif sw_d1 /= cmdvec(8) then
          cmdvec(8) <= sw_d1;
        end if;
      end if;
    when s1_sendcmd => -- create output for PGA chain
      bit_index <= bit_index - '1';
      --create command word
      --RIGHT
      cmdvec(31) <= '0'; -- ~DC servo ena
      cmdvec(30) <= '1'; -- CM servo
      cmdvec(29) <= '0'; -- placeholder
      cmdvec(28) <= '1'; -- overload 0 = 5.1 Vrms 1 = 4.0 Vrms
      cmdvec(27) <= '0'; -- GFO4
      cmdvec(26) <= '0'; -- GFO3
      cmdvec(25) <= '0'; -- GFO2
      -- cmdvec(24) <= sw d1;-- GFO1
  end case;
cmdvec(23) <= '0'; -- placeholder
kmdvec(22) <= '0'; -- placeholder
kmdvec(21 downto 16) <= CONV_STD_LOGIC_VECTOR(gainR, 6); -- gain

--LEFT
kmdvec(15) <= '0'; -- ~DC servo ena
kmdvec(14) <= '1'; -- CN servo
kmdvec(13) <= '0'; -- placeholder
kmdvec(12) <= '1'; -- overload 0 = 5.1 Vrms 1 = 4.0 Vrms
kmdvec(11) <= '0'; -- GPO4
kmdvec(10) <= '0'; -- GPO3
kmdvec(9)  <= '0'; -- GPO2
-- cmdvec(8) <= sw_d1; -- GPO1
kmdvec(7)  <= '0'; -- placeholder
kmdvec(6)  <= '0'; -- placeholder
kmdvec(5 downto 0) <= CONV_STD_LOGIC_VECTOR(gainL, 6); -- gain

END CASE;

END IF;

END PROCESS;

PROCESS (currentState, bit_index, db_pb_up, db_pb_dn, sw_d1, pb_gainzero, cmdvec)
BEGIN

nextState <= currentState;
if(currentState = s0_chkPBS) then
  pga_sdo <= '0';
  pga_cs <= '1';
  IF (pb_gainzero = '0') or (db_pb_up = '0') or (db_pb_dn = '0') THEN
    nextState <= s1_sendcmd;
  ELSEIF sw_d1 /= cmdvec(8) THEN
    nextState <= s1_sendcmd;
  END IF;
else -- currentState = s1_sendcmd -- send output to PGA chain
  IF (bit_index = "0000") then
    nextState <= s0_chkPBS;
  end if;
  pga_cs <= '0';
  pga_sdo <= cmdvec(conv_integer(bit_index));
end if;
END PROCESS;
end architecture;

Flow Status Successful - Thu May 05 02:16:34 2005
Revision Name pga_bst
Top level Entity Name pga_bst
Family MAX3000A
Device EPM3064AFLC44-10
Timing Models Final
Met timing requirements Yes
Total macrocells 54 / 64 (100 %)
Total pins 21 / 34 (61 %)
Control Logic prototype circuit
### Economic Analysis

#### INCOME STATEMENT OVER A FIVE YEAR PERIOD

<table>
<thead>
<tr>
<th></th>
<th>YEAR 1</th>
<th>YEAR 2</th>
<th>YEAR 3</th>
<th>YEAR 4</th>
<th>YEAR 5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Estimated Quantity sold</td>
<td>1000000</td>
<td>1250000</td>
<td>1562500</td>
<td>1953125</td>
<td>2441406</td>
</tr>
<tr>
<td>Selling price per item</td>
<td>200</td>
<td>180</td>
<td>160</td>
<td>140</td>
<td>120</td>
</tr>
<tr>
<td>Sales Revenue</td>
<td>200000000</td>
<td>225000000</td>
<td>250000000</td>
<td>273437500</td>
<td>292968750</td>
</tr>
<tr>
<td>Cost of parts per item</td>
<td>6000000</td>
<td>7500000</td>
<td>9375000</td>
<td>117187500</td>
<td>146484375</td>
</tr>
<tr>
<td>Manufacturing Cost</td>
<td>3000000</td>
<td>3750000</td>
<td>4687500</td>
<td>5859375</td>
<td>7324219</td>
</tr>
<tr>
<td>Cost of rework</td>
<td>4500000</td>
<td>5625000</td>
<td>7031250</td>
<td>8789063</td>
<td>10986328</td>
</tr>
<tr>
<td>Gross Margin</td>
<td>132500000</td>
<td>140625000</td>
<td>144531250</td>
<td>141601563</td>
<td>128173828</td>
</tr>
<tr>
<td>Selling expenses</td>
<td>50000000</td>
<td>62500000</td>
<td>78125000</td>
<td>97656250</td>
<td>122070313</td>
</tr>
<tr>
<td>Earnings before Tax</td>
<td>82500000</td>
<td>78125000</td>
<td>66406250</td>
<td>43945313</td>
<td>6103516</td>
</tr>
<tr>
<td>Tax (12%)</td>
<td>9900000</td>
<td>9375000</td>
<td>7968750</td>
<td>5273438</td>
<td>732422</td>
</tr>
<tr>
<td>Total Cost of product</td>
<td>127400000</td>
<td>156250000</td>
<td>191562500</td>
<td>234765625</td>
<td>287597656</td>
</tr>
<tr>
<td>Present Value Interest Factor (12%)</td>
<td>0.8929</td>
<td>0.7972</td>
<td>0.7118</td>
<td>0.6355</td>
<td></td>
</tr>
<tr>
<td>Present value (of total cost)</td>
<td>$127,400,000</td>
<td>$139,515,625</td>
<td>$152,713,625</td>
<td>$167,106,172</td>
<td>$182,768,311</td>
</tr>
<tr>
<td>Net Present Value (of total cost)</td>
<td>$769,503,732</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Net Income</td>
<td>$72,600,000</td>
<td>$68,750,000</td>
<td>$58,437,500</td>
<td>$38,671,875</td>
<td>$5,371,094</td>
</tr>
<tr>
<td>Present Value (of income)</td>
<td>$72,600,000</td>
<td>$61,386,875</td>
<td>$46,586,375</td>
<td>$27,526,641</td>
<td>$3,413,330</td>
</tr>
<tr>
<td>Net Present Value (of income)</td>
<td>$211,513,221</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Return on investment</td>
<td>0.274869649</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 2: Income statement over a five year period

N/B

Estimated quantity sold

Sales revenue = row 5 * row 4

Selling price in selling price

Cost of parts per item = row 5 * row 4

Battery ($15), Analog signal path ($20), USB parts ($20), packaging ($5), total = $60

Manufacturing cost = $3 * row 4

Cost of rework = 15% of row 4 * $30

Gross margin = Row 6 - row 7 - row 8

Selling expenses = $50 * row 4

Earnings b/tax = row 9 - row 10

Tax = 12% of row 11

Total cost of production = rows (7+8+10+12)

Net income = row 11 - row 12
## Power Requirements

<table>
<thead>
<tr>
<th>POWER REQUIREMENTS</th>
<th>Recommended Converter / regulator</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Preamp</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply voltage, VA+ = +5.5V</td>
<td>TPS70102</td>
<td>Dual-Output Low-Dropout (LDO) Voltage Regulator with Power Up Sequencing For Split Vo</td>
</tr>
<tr>
<td>Supply voltage, VA- = -5.5V</td>
<td>UC3572</td>
<td>Negative Output Flyback Pulse Width Modulator</td>
</tr>
<tr>
<td>Supply voltage, VD- = -5.5V</td>
<td>UC3572</td>
<td>Negative Output Flyback Pulse Width Modulator</td>
</tr>
<tr>
<td>Analog input voltage (VA-) -0.3V to (VA+) 0.3V</td>
<td>TPS54372</td>
<td>3-A Active Bus Termination/ DDR Memory DC/DC Converter</td>
</tr>
<tr>
<td>Phantom power = +48VDC</td>
<td>H5</td>
<td>Inputs 5-15, 9-36, 20-60Vdc and outputs 24Vdc to 1000Vdc and power = 5W</td>
</tr>
<tr>
<td><strong>ADC</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply voltage = +6V analog</td>
<td>LM317L</td>
<td>3-Terminal, 100mA Adjustable Positive Voltage Regulator</td>
</tr>
<tr>
<td>Supply voltage = +3.6V digital</td>
<td>TPS70102</td>
<td>Dual-Output Low-Dropout (LDO) Voltage Regulator with Power Up Sequencing For Split Vo</td>
</tr>
<tr>
<td><strong>Digital Line Driver</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply voltage = +6.5V</td>
<td>LM3478</td>
<td>SoftStart, Adj. Peak Current Limit</td>
</tr>
<tr>
<td>Digital input voltage = 0.2V to +5.5V</td>
<td>TPS70102</td>
<td>Dual-Output Low-Dropout (LDO) Voltage Regulator with Power Up Sequencing For Split Vo</td>
</tr>
<tr>
<td><strong>Sample Rate Converter</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply voltage = +3.3V</td>
<td>TPS71533</td>
<td>50-mA, 3.3-V High Input-Voltage LDO Voltage Regulator in SC-70</td>
</tr>
<tr>
<td><strong>USB Board</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Voltage = +15V</td>
<td>PT5042</td>
<td>15Vout 0.75A 5V-Input Step-Up ISR</td>
</tr>
<tr>
<td>6V rechargeable battery</td>
<td>6V 1200mAh NiMH BEC Battery Pack</td>
<td>6V rechargeable battery which have high capacity and no memory effect</td>
</tr>
</tbody>
</table>
48V Phantom power design

48V DC-DC converter schematic

Figure 6.6.2: 6 to 48V DC-DC boost converter from http://www.national.com/
# 48V DC-DC converter parts list

<table>
<thead>
<tr>
<th>Part</th>
<th>Manufacturer</th>
<th>Part#</th>
<th>Attributes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cbyp</td>
<td>Vishay Vitramon</td>
<td>VJ0805Y104KXXA</td>
<td>0.1u F</td>
</tr>
<tr>
<td>Comp</td>
<td>Vishay Vitramon</td>
<td>VJ0805Y104KXXA</td>
<td>0.1u F</td>
</tr>
<tr>
<td>Cin</td>
<td>Vishay Sprague</td>
<td>595D227X9010R2</td>
<td>NumCaps=1 220u F,130m Ohms</td>
</tr>
<tr>
<td>Cout</td>
<td>Vishay Sprague</td>
<td>595D157X9016R2</td>
<td>NumCaps=1 150u F,130m Ohms</td>
</tr>
<tr>
<td>Csense</td>
<td>Vishay Vitramon</td>
<td>VJ0805Y103KXXA</td>
<td>0.01u F</td>
</tr>
<tr>
<td>D1</td>
<td>ON Semiconductor</td>
<td>MBRS340T3</td>
<td>0.525 V</td>
</tr>
<tr>
<td>IC</td>
<td>National Semiconductor</td>
<td>M3478MM</td>
<td></td>
</tr>
<tr>
<td>L1</td>
<td>Coilcraft</td>
<td>DO3316P-332</td>
<td>3.3u H,15m Ohms</td>
</tr>
<tr>
<td>M1</td>
<td>Fairchild</td>
<td>FDS6690A</td>
<td>1.2n ,17m</td>
</tr>
<tr>
<td>Rcomp</td>
<td>Vishay Vitramon</td>
<td>CRCW08051001</td>
<td>1k Ohms</td>
</tr>
<tr>
<td>Rdr</td>
<td>Vishay Vitramon</td>
<td>CRCW0805600R0</td>
<td>1u Ohms</td>
</tr>
<tr>
<td>Rfadj</td>
<td>Vishay Vitramon</td>
<td>CRCW08054022</td>
<td>40.2k Ohms</td>
</tr>
<tr>
<td>Rfb1</td>
<td>Vishay Vitramon</td>
<td>CRCW00051002</td>
<td>10k Ohms</td>
</tr>
<tr>
<td>Rfb2</td>
<td>Vishay-Dale</td>
<td>CRCW1206-3743FRT1</td>
<td>3.74e+05 Ohms</td>
</tr>
<tr>
<td>Rs1</td>
<td>Vishay Vitramon</td>
<td>CRCW08056040</td>
<td>604 Ohms</td>
</tr>
<tr>
<td>Rsense</td>
<td>Custom</td>
<td>Custom</td>
<td>0.03825 Ohms</td>
</tr>
</tbody>
</table>
### USB source code

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Size (KB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>app.c</td>
<td>Main application file.</td>
<td>44</td>
</tr>
<tr>
<td>app.d</td>
<td>Compiler file - Main application.</td>
<td>1</td>
</tr>
<tr>
<td>app.h</td>
<td>Header file - Main application.</td>
<td>8</td>
</tr>
<tr>
<td>ask_confirmation.d</td>
<td>Compiler file.</td>
<td>1</td>
</tr>
<tr>
<td>bios_idle.d</td>
<td>Compiler file - BIOS.</td>
<td>0</td>
</tr>
<tr>
<td>board.d</td>
<td>Compiler file - Board.</td>
<td>1</td>
</tr>
<tr>
<td>check_sizes</td>
<td>Debug file - Memory allocation.</td>
<td>1</td>
</tr>
<tr>
<td>check_sizes.awk</td>
<td>Debug file - Memory allocation.</td>
<td>2</td>
</tr>
<tr>
<td>check_sizes.d</td>
<td>Compiler file - Memory allocation.</td>
<td>1</td>
</tr>
<tr>
<td>clean</td>
<td>Compiler file - Clean up utility.</td>
<td>1</td>
</tr>
<tr>
<td>console.d</td>
<td>Compiler file - Console.</td>
<td>1</td>
</tr>
<tr>
<td>cy_itoa.d</td>
<td>Compiler file - Processor.</td>
<td>1</td>
</tr>
<tr>
<td>cy_printf.d</td>
<td>Compiler file - Processor.</td>
<td>1</td>
</tr>
<tr>
<td>dealloc_all_devices.d</td>
<td>Compiler file - Deallocate all devices.</td>
<td>1</td>
</tr>
<tr>
<td>debug.d</td>
<td>Compiler file - Debug.</td>
<td>1</td>
</tr>
<tr>
<td>device.d</td>
<td>Compiler file - Device.</td>
<td>1</td>
</tr>
<tr>
<td>disable_serial_dbg.d</td>
<td>Compiler file - Disable serial port.</td>
<td>0</td>
</tr>
<tr>
<td>drvlist.h</td>
<td>Header file - Driver list.</td>
<td>3</td>
</tr>
<tr>
<td>fat.d</td>
<td>Compiler file - FAT file system.</td>
<td>1</td>
</tr>
<tr>
<td>fat_findfirst.d</td>
<td>Compiler file - FAT file system.</td>
<td>1</td>
</tr>
<tr>
<td>fat_getlabel.d</td>
<td>Compiler file - FAT file system.</td>
<td>1</td>
</tr>
<tr>
<td>fat_is_valid_path.d</td>
<td>Compiler file - FAT file system.</td>
<td>1</td>
</tr>
<tr>
<td>fat_setlabel.d</td>
<td>Compiler file - FAT file system.</td>
<td>1</td>
</tr>
<tr>
<td>filesystem.d</td>
<td>Compiler file - FAT file system.</td>
<td>1</td>
</tr>
<tr>
<td>fs.access.d</td>
<td>Compiler file - FAT file system.</td>
<td>1</td>
</tr>
<tr>
<td>fs.chdir.d</td>
<td>Compiler file - FAT file system.</td>
<td>1</td>
</tr>
<tr>
<td>fs_chdrive.d</td>
<td>Compiler file - FAT file system.</td>
<td>1</td>
</tr>
<tr>
<td>fs_close.d</td>
<td>Compiler file - 'close' command.</td>
<td>1</td>
</tr>
<tr>
<td>fs_commit.d</td>
<td>Compiler file - 'commit' command.</td>
<td>1</td>
</tr>
<tr>
<td>fs_create.d</td>
<td>Compiler file - 'create' command.</td>
<td>1</td>
</tr>
<tr>
<td>fs_drvlist.h</td>
<td>Compiler file - 'drvlist' command.</td>
<td>3</td>
</tr>
<tr>
<td>fs_eof.d</td>
<td>Compiler file - 'eof' command.</td>
<td>1</td>
</tr>
<tr>
<td>fs_findfirst.d</td>
<td>Compiler file - 'findfirst' command.</td>
<td>1</td>
</tr>
<tr>
<td>fs_format.d</td>
<td>Compiler file - 'format' command.</td>
<td>1</td>
</tr>
<tr>
<td>fs_getcwd.d</td>
<td>Compiler file - 'getcwd' command.</td>
<td>1</td>
</tr>
<tr>
<td>fs_getdrive.d</td>
<td>Compiler file - 'getdrive' command.</td>
<td>1</td>
</tr>
<tr>
<td>fs_gettime.</td>
<td>Compiler file - '_gettime' command.</td>
<td>1</td>
</tr>
<tr>
<td>fs_open.d</td>
<td>Compiler file - 'open' command.</td>
<td>1</td>
</tr>
<tr>
<td>fs_remove.d</td>
<td>Compiler file - 'remove' command.</td>
<td>1</td>
</tr>
<tr>
<td>fs_rename.d</td>
<td>Compiler file - 'rename' command.</td>
<td>1</td>
</tr>
<tr>
<td>fs_rmdir.d</td>
<td>Compiler file - 'rmdir' command.</td>
<td>1</td>
</tr>
<tr>
<td>fs_sethandle.</td>
<td>Compiler file - 'sethandle' command.</td>
<td>1</td>
</tr>
<tr>
<td>fs_setlabel.d</td>
<td>Compiler file - 'setlabel' command.</td>
<td>1</td>
</tr>
<tr>
<td>fs_tell.d</td>
<td>Compiler file - 'tell' command.</td>
<td>1</td>
</tr>
<tr>
<td>fs_write.d</td>
<td>Compiler file - 'write' command.</td>
<td>1</td>
</tr>
<tr>
<td>fullpath.d</td>
<td>Compiler file.</td>
<td>1</td>
</tr>
</tbody>
</table>